REMARKS

Claims 1, 3-13, and 15-18 are pending. Claims 2 and 14 have been canceled and claims 1, 3, 4, 6, 10, 13, 15, and 16 have been amended. Reconsideration and allowance of the present application based on the above amendments and the following remarks are respectfully requested.

In the Specification

The abstract and specification is objected to for containing the term ladder-like, which the Examiner alleges is vague. Applicant has amended the specification and abstract in accordance with the Examiner's suggestion, by replacing the term "ladder-like" with --ladder-shaped--. Additionally, the Examiner has objected to the use of the phase "formed at a less depth". In accordance with the Examiner's suggestion, Applicant has amended the abstract to replace the phrase "formed at a less depth" with --formed at a shallower depth--. Therefore, Applicant respectfully submits that this objection is obviated.

Claim Objections

1. Claims 1-12 are objected to for informalities. Specifically, with regard to claim 1, the Examiner indicates several areas the require clarification and proposes amendments that will clarify claim 1. Applicant has amended claim 1 for clarity only in accordance with the Examiner's suggestion. Accordingly, Applicant respectfully submits that this objection is obviated.

2. Claims 2, 3, 6, 7, 10, 11, 14, and 15 are objected under 37 C.F.R. 1.75(b) for being of improper dependant form. Specifically, the Examiner indicates that claims 2 and 14, which depend from claims 1 and 13 respectively, do not further limit the subject matter of the claims from which they depend. In accordance with the Examiner's suggestion, Applicant has cancelled claims 2 and 14 and their subject matter has been incorporated into claims 1 and 13, respectively, for increased breadth. Additionally, claims 3, 6, 10, and 15 have been amended to depend from claim 1. Therefore, Applicant respectfully submits that this objection is obviated.

3. Claims 13-18 are objected to for informalities. Specifically, with regard to claim 13, the Examiner indicates several areas that require clarification and proposes amendments that

will clarify claim 13. Applicant has amended claim 13 for clarity only in accordance with the Examiner's suggestion. Accordingly, Applicant respectfully submits that this objection is obviated.

4. Claims 4 and 16 are objected to because of informalities. Specifically, as discussed above, the term ladder-like is allegedly indefinite. Accordingly, as proposed by the Examiner, Applicant has amended claims 4 and 16 for clarity only to change the "ladder-like" to --ladder-shaped--. Therefore, Applicant respectfully submits that this objection is obviated.

Conclusion

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

Pillsbury Winthrop LLP

By: _____

Paul T. Bowen
Reg. No.:38009
Tel. No.: (703) 905-2020
Fax No.: (703) 905-2500

PTB\VXK
1600 Tysons Boulevard
McLean, VA 22102

(703) 905-2000
Enclosure: Appendix
Abstract

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning on page 1, line 20 and ending on page 2, line 3 has been amended as follows:

As a power semiconductor device, an insulated gate bipolar transistor (IGBT) in which N-type emitters formed in contact with trench gates are connected by N-type semiconductor regions so as to form a [ladder-like] ladder-shaped configuration has been proposed (e.g., in Japanese Patent Application Laid-Open No. HEI 9-270512). In this device, the emitter-contact width is reduced by forming [ladder-like] ladder-shaped N-type semiconductor regions. In this device, the N-type emitters and the N-type semiconductor regions are formed by a single diffusion layer, and therefore, their depths are substantially equal.

The paragraph beginning on page 4, line 20 and ending on page 5, line 26 has been amended as follows:

The power semiconductor device 20 of this embodiment, as shown in the drawings, has a body 24 of a P^--type semiconductor region formed on a surface of an N^--type epitaxial layer 22 that is formed on a substrate 21 formed by a P-type or N-type semiconductor. A plurality of trench gates 26 are disposed parallel to one another and extend from an obverse surface, which in FIGURE 1 is the top surface, of a semiconductor substrate through the body 24 to the epitaxial layer 22. Formed on opposite sides of each trench gate 26 are emitter regions that are N^+-type semiconductor regions contacting the trench gate 26 via a gate-insulating film 27, such as a silicon oxide film or the like. In this embodiment, the emitter regions are formed by trench-emitter regions 28 (a first semiconductor region) and emitter-connecting regions 30 (a second semiconductor region). The emitter-connecting regions 30 connect trench-emitter regions 28 that face each other so as to form a [ladder-like] ladder-shaped configuration. The power semiconductor device 20 further has contact P regions 32 that are P^+-type semiconductor regions formed between the emitter-connecting regions 30 on the body 24. The power semiconductor device 20 may be a power MOSFET (where the substrate 21 is of N-type), an insulated gate bipolar transistor (IGBT, where the substrate 21 is of P-type) which is a generally-termed vertical-type device wherein a main current flows in a vertical direction with respect to the substrate, or a composite device that partially has a

construction of a device mentioned above. FIGURES 1 and 2 show design pattern for the power semiconductor device 20. The contact P region 32 and the trench-emitter regions 28 can be formed by thermal diffusion. Therefore, in a practical manner, a part of the contact P region 32 and a part of the trench-emitter regions 28 may overlap each other.

IN THE CLAIMS:

Claims 2 and 14 have been canceled and claims 1, 3, 4, 6, 10, 13, 15, and 16 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a body region of a first conductivity type formed in a semiconductor substrate and having a major surface opposite to the surface shared between the semiconductor substrate and the body region;

a plurality of trench gates extending through the body region;

a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from [a] said major surface of the body region [and sandwiching], at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via [the gate-insulating] films bordering and insulating the trench gates; and

a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from [the] said major surface of the body region that is less than the first depth,

wherein the second semiconductor regions connect the plurality of first semiconductor regions spaced apart from one another.

3. (Amended) A semiconductor device according to claim [2] 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

4. (Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a [ladder-like] ladder-shaped configuration.

6. (Amended) A semiconductor device according to claim [2] 1, further comprising a wiring member connected to at least one of the plurality of trench gates.

10. (Amended) A semiconductor device according to claim [2] 1, further comprising a wiring member connected to the body region and to the second semiconductor region.

13. (Amended) A process for producing a semiconductor device comprising:

forming a body region of a first conductivity type in a semiconductor substrate, the body region having a major surface opposite to the surface shared between the semiconductor substrate and the body region;

forming a plurality of trench gates extending through the body region;

forming a plurality of first semiconductor regions of a second conductivity type that is different from the first conductivity type, the first semiconductor regions having a first depth as measured from [a] said major surface of the body region [and sandwiching], at least a portion of the first semiconductor regions flanking the trench gates on both of their sides and being in contact with said trench gates via [gate-insulating] films bordering and insulating the trench gates;

forming a plurality of second semiconductor regions of the second conductivity type having a second depth as measured from [the] said major surface of the body region that is less than the first depth; and

connecting the plurality of first semiconductor regions spaced apart from one another by the second semiconductor regions.

15. (Amended) A process according to claim [14] 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a ladder-like configuration.

16. (Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a [ladder-like] ladder-shaped configuration.

IN THE ABSTRACT:

The Abstract of the disclosure has been amended as follows:

A power semiconductor device having a low on-resistance and a high breakdown ruggedness is disclosed. Trench regions formed so as to contact trench gates via gate-insulating films are connected by emitter regions so as to form a [ladder-like] ladder-shaped configuration. The emitter regions are formed at a [less] shallower depth than the trench regions. Therefore, the resistance in portions of the body that are near the interfaces with the emitter regions is reduced, and the operation of parasitic transistors formed by the emitter regions, the body, and an epitaxial layer is substantially prevented. As a result, the on-resistance is varied, and the avalanche ruggedness and the latch-up ruggedness are improved.